

FINAL YEAR PROJECT REPORT

**IMPLEMENTATION OF QUADRATURE DIRECT DIGITAL FREQUENCY  
SYNTHESIZER (QDDFS) USING FPGA**



Submitted by

Abdullah AizazDodhy (111619-267)

WaqarShahzad (111619-203)

Abad ul Hassan (111619-213)

Submitted in partial fulfillment of the requirements for the degree

**BACHELORS OF ELECTRICAL ENGINEERING**

APPROVED

Project Advisor: \_\_\_\_\_

Director Projects: \_\_\_\_\_

DEPARTMENT OF ELECTRICAL ENGINEERING  
SCHOOL OF ENGINEERING  
UNIVERSITY OF MANAGEMENT AND TECHNOLOGY  
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## DECLARATION

We declare that this project entitled, "**Implementation of Quadrature Direct Digital Frequency Synthesizer (QDDFS) Using FPGA**" submitted to the "Department Of Electrical Engineering" under School Of Engineering at University Of Management And Technology, is the record and written evidence of our work under the guidance of Mr. Muhammad Asim Butt (Assistant Professor at Electrical Engineering Department). This project is submitted in the partial fulfillment of the requirements to award the degree of Bachelors of Science in Electrical Engineering. The results in this document do not contain any material which has been previously submitted for a degree to any university as per our knowledge.

Abdullah AizazDodhy

Signature: \_\_\_\_\_

WaqarShahzad

Signature: \_\_\_\_\_

Abad ul Hassan

Signature: \_\_\_\_\_

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## **ABSTRACT**

**This thesis is basically the implementation of quadrature direct digital frequency synthesizer (QDDFS) which is one of the main building blocks used in software defined radios (SDR). The implementation of the DDFS computes the sine and cosine function on a single edge of the clock, proving it to be optimized in terms of area and speed. The actual architecture which can be offered in the papers is better than CO-ordinate Rotation Digital Computer (CORDIC) as well as Singleton's offered architecture. Complete designing procedure is explained in the report for better understanding the operation of Direct Digital Frequency Synthesizer. All the computations are performed using Q m.n fixed number representation system. Fixed-Point implementation was accomplished using ModelSim simulator. Verilog HDL is a Hardware descriptive language and is used as a description language to map different algorithms. Artix-7 Field Programmable Gate Array (FPGA) Nexys-4 by Digilent is chosen as a Hardware Platform for the System Implementation.**

# Table of Contents

<i>Chapter</i>		<i>1</i>					
<i>Introduction</i> .....							<i>4</i>
<i>Chapter</i>	<i>2</i>	<i>-</i>					<i>Theoretical</i>
<i>background</i> .....							<i>5</i>
<i>2.1-</i>	<i>Direct</i>	<i>Digital</i>					<i>Frequency</i>
<i>synthesizer</i> .....							<i>5</i>
<i>2.2-</i>							<i>Mathematical</i>
<i>Calculations</i> .....							<i>8</i>
<i>2.3-</i>							<i>Output</i>
<i>Frequency</i> .....							<i>9</i>
<i>2.4-</i>	<i>Proposed</i>	<i>Architecture</i>					<i>of</i>
<i>QDDFS</i> .....							<i>Error! Bookmark not defined.1</i>
<i>2.5-</i>							<i>Problems</i>
<i>Encountered</i> .....							<i>Error!</i>
<i>Bookmark not defined.2</i>							
<i>Chapter</i>	<i>3</i>	<i>-</i>	<i>Architecture</i>	<i>Simulation</i>			<i>and</i>
<i>Impementation</i> .....							<i>17</i>
<i>3.1-</i>	<i>Software</i>	<i>Implementation</i>		<i>using</i>	<i>Xilinx</i>		<i>ISE</i>
<i>14.3</i> .....							<i>17</i>
<i>3.2-</i>	<i>Simulation</i>			<i>of</i>			<i>a</i>
<i>Project</i> .....							<i>23</i>
<i>3.3-</i>	<i>Implementation</i>			<i>of</i>			<i>a</i>
<i>Project</i> .....							<i>25</i>
<i>Chapter</i>	<i>4</i>	<i>-</i>	<i>Theoretical</i>	<i>details</i>	<i>of</i>		<i>building</i>
<i>blocks</i> .....							<i>26</i>
<i>4.1-</i>	<i>Module</i>			<i>of</i>			<i>8-bit</i>
<i>Adder</i> .....							<i>26</i>
<i>4.2-</i>	<i>Module</i>			<i>of</i>			<i>8-bit</i>
<i>Multiplier</i> .....							<i>27</i>
<i>4.3-</i>	<i>Module</i>			<i>of</i>			<i>8-bit</i>
<i>Multiplexer</i> .....							<i>28</i>
<i>4.4-</i>	<i>Module</i>			<i>of</i>			<i>8-bit</i>
<i>Register</i> .....							<i>29</i>
<i>4.5-</i>	<i>Module</i>			<i>of</i>			<i>8-bit</i>
<i>TOP</i> .....							<i>30</i>
<i>Chapter</i>	<i>5</i>	<i>-</i>					<i>Hardware</i>
<i>Implementation</i> .....							<i>32</i>
<i>5.1-</i>							<i>FPGA</i>
.....							<i>32</i>
<i>5.2-</i>			<i>Vendors</i>				<i>of</i>
<i>FPGA</i> .....							<i>32</i>

<i>Chapter</i>	<i>6</i>	<i>-</i>	<i>FMC</i>	<i>/</i>	<i>DAC</i>
<i>Card</i> .....					<i>33</i>
<i>6.1-</i>	<i>FPGA</i>		<i>Mezzanine</i>		<i>Card</i>
<i>(FMC)</i> .....					<i>33</i>
<i>6.2-</i>	<i>Xilinx</i>	<i>Artix</i>	<i>7</i>	<i>AC701</i>	<i>Evaluation</i>
<i>kit</i> .....					<i>34</i>
<i>6.3-</i>	<i>Digital</i>	<i>to</i>	<i>Analog</i>		<i>Converter</i>
<i>(DAC)</i> .....					<i>35</i>
<i>Verilog</i>					<i>Code</i>
.....					<i>36</i>
<i>References</i>					
.....					<i>40</i>

## List of Figures

Figure 1.1	General diagram of FPGA with DAC card .....	4
Figure 2.1	Diagram of Phase lock loop (PLL).....	5
Figure 2.2	Direct Analog Synthesis .....	6
Figure 2.3	Direct Digital Frequency synthesizer .....	6
Figure 2.4	Proposed Architecture of QDDFS.....	11
Figure 2.5-7	Simulations in Modelsim .....	14-16
Figure 3.1-3.15	From Synthesis to Implementation using Xilinx ISE 14.3.....	18-25
Figure 4.1-6	RTL Schematic Diagram of the project.....	26-31
Figure 5.1	Diagram of building blocks of FPGA .....	32
Figure 6.1	Diagram of FPGA Mezzanine Card.....	33
Figure 6.2	Diagram of Artix 7 Evaluation Board Xilinx.....	34
Figure 6.3-4	Digital to analog converter.....	35-36

