FINAL YEAR PROJECT REPORT

DESIGN OF DIGITAL SYNCHRONISM CHECKING RELAY FOR INTERCONNECTED POWER GRIDS

Project Advisor
Mr. Asif Hussain

Submitted by

Mudassar Iqbal	081220161
Muhammad Sohaib Saad	081220203
Shahid Farooq	081220033

DEPARTMENT OF ELECTRICAL ENGINEERING
SCHOOL OF SCIENCE AND TECHNOLOGY
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Design of Digital Synchronism Checking Relay for Interconnected Power Grids

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In

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Mudassar Iqbal	081220161
Muhammad Sohaib Saad	081220203
Shahid Farooq	081220033

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Abstract

In this project we have designed a circuit to connect to parts of interconnected system energized by two different sources. By interconnecting separate utilities with the high voltage transmission system, it is possible to pool both generation and demand, not only providing a number of economic and other benefits, including a more efficient bulk transfer of power from generation to demand centers. The interconnected transmission system, by linking together all participants across the transmission system, makes it is possible to select the cheapest generation available. Transmission circuits tend to be far more reliable than individual generating units, and enhanced security of supply is achieved because the transmission system is better able to exploit the diversity between individual generation sources and demand. An interconnected transmission system enables surplus generation capacity in one area to be used to cover shortfalls elsewhere on the system, resulting in lower requirements for additional installed generation capacity, to provide sufficient generation security for the whole system. Without transmission interconnection, each separate system would need to carry its own frequency response to meet demand variations, but with interconnection the net response requirement only needs to match the highest of the individual system requirements to cover for the largest potential loss of power (generation) rather than the sum of them all.

Main idea is to calculate voltage, frequency and phase angle of both sides using digital sampling and compare these values. If they lie in tolerable range then permission to close command is issued for respective circuit breaker.

High performancePIC18F452 RISC CPU is used for processing the inputs. Sinusoidal signals from both ends of system are converted to digital form and after half wave rectification these samples are used for calculation of voltage. To measure frequency input sine wave is converted to square wave and then positive edge triggered external interrupts are used to count the number of cycles in one second.

Measuring phase angle was quite an interesting task and caused a lot of effort. Time difference between starting of two waves is used to compute phase angle.

Monitoring the system using synchro check relay before synchronization of supplies for the confidence of utility can save from a lot of trouble caused by out of step trippings.

Dedication

This Research Paper is lovingly dedicated to our respective parents who have been our constant source of inspiration. They have given us the drive and discipline to tackle any task with enthusiasm and determination. Without their love and support this project would not have been made possible.

Acknowledgements

First of all we are very thankful to ALLAH who gave us strength and courage to complete this project.

We have taken efforts in this project. However, it would not have been possible without the kind support and help of many individuals and organizations. We would like to extend our sincere thanks to all of them.

We are highly indebted to Faculty of University of Management and Technology for their guidance and constant supervision as well as for providing necessary information regarding the project & also for their support in completing the project.

We would like to express our gratitude towards our teachers for their kind co-operation and encouragement which help us in completion of this project.

We would like to express our special gratitude and thanks to Mr. Asif Hussain, Mr Rauf Ali and Mr. Saleem Ata for supporting us with their precious time.

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TABLE OF CONTENTS

LIST OF FIGURES

CHAPTER I - INTRODUCTION

In modern power systems generators are operated in parallel to increase the efficiency of system. Parallel operation of AC generators causes easy handling of larger loads due to reactive power sharing capability of interconnected grid. It can absorb harmonics caused by switching of major loads. A large sum of capital is saved to increased cost efficiency thanks to economically dispatched distributed generation systems. Maintenance was big issue in power system before the concept of parallel generation and it often caused large blackout for long times. Nowadays whole system is connected in such a way that multiple paths are always available for power flow. This takes the system to a whole new level of dependability with total peace of mind.

1.1 PROBLEM STATEMENT

Paralleling of two or more generators requires some basic condition to be satisfied otherwise it may damage the generator or system. These conditions are:

a) Line voltages must be equal.

b) The generators to be paralleled must have the same phase sequence.

c) Generator output phase angles must be the same.

d) The oncoming generator (the new generator) must have a slightly higher operating frequency as compared to the system frequency.

The main objective of our project is to connect a generator to the system. Applications of our work include:

- Re-establishing the connection between two parts of the system.
- Closing ring mains and interconnecting busbars.
- Manual closing of circuit breakers
- Automatic reclosing of a breaker after a relay trip.

1.2 SCOPE OF WORK

Upon completion of project we will be able to present a digital synchronism-checking relay that will measure bus and line voltages and provide an output to enable the closing of circuit breaker when all of the values fall within the set limits and remain there for the duration selected in the setting. It will test:

- Voltage difference
- Frequency slip
- The phase angle between both voltages

1.3 PROJECT METHODOLOGY

Synchronism check is intended primly for application where the two parts of a system to be joined by the closure of a circuit breaker. Usually, performing synchronism check measurements is done with relatively long times in order to make sure the voltages are synchronized. Nevertheless, this long timer, which can be on the order of 10 to 20 seconds, is not appropriate when both ends of the line are to be reclosed at high speed. If the measurement time is lower, then the synchronism check can be done faster, although this means that the reclosing could be done under no-synchronism conditions, with greater frequency slip than for ideal condition. Once the basic fundamental magnitudes and their derivatives have been obtained, they are compared to the settings. The frequency slip, which has to be less than that specified, configures a very basic condition of closure, optimum for carrying out closure procedures in ideal conditions, with similarity between signals.

Measurement will be obtained via a numerical calculation done on digital voltage samples. Given that in power systems, synchronization or synchronism checking is carried out in a steady state, that is with voltage magnitudes near or equal to the rated value, close enable is not emitted for very low voltages.

1.4 SOFTWARE USED

1.4.1 PCW IDE Compiler for Microchip PIC®

CCS provides a complete, integrated tool suite for developing and debugging embedded applications running on Microchip PIC® MCUs and dsPIC® DSCs. This suite includes an IDE for project management, a context sensitive C aware editor, build tools and real time debugger...helping developers create, analyze, debug and document project code.

The CCS IDE allows developers to manage every aspect of their embedded software development, from code creation through device programming. External programs can be invoked from the IDE, simplifying integration with other programmers and debuggers.

The heart of this development tool suite is the CCS intelligent code optimizing C compiler, which frees developers to concentrate on design functionality instead of having to become an MCU architecture expert. Maximize code reuse by easily porting from one MCU to another. Minimize lines of new code with CCS provided peripheral drivers, built-in functions and standard C operators. Built in libraries are specific to PIC® MCU registers, allowing access to hardware features directly from C.

1.4.2 PROTEUS

1.4.2.1 The VSM Advantage

The Proteus Design Suite is wholly unique in offering the ability to co-simulate both high and low-level micro-controller code in the context of a mixed-mode SPICE circuit simulation. With this Virtual System Modeling facility, you can transform your product design cycle, reaping huge rewards in terms of reduced time to market and lower costs of development.

If one person designs both the hardware and the software then that person benefits as the hardware design may be changed just as easily as the software design. In larger organizations where the two roles are separated, the software designers can begin work as soon as the schematic is completed; there is no need for them to wait until a physical prototype exists.

In short, Proteus VSM improves efficiency, quality and flexibility throughout the design process.

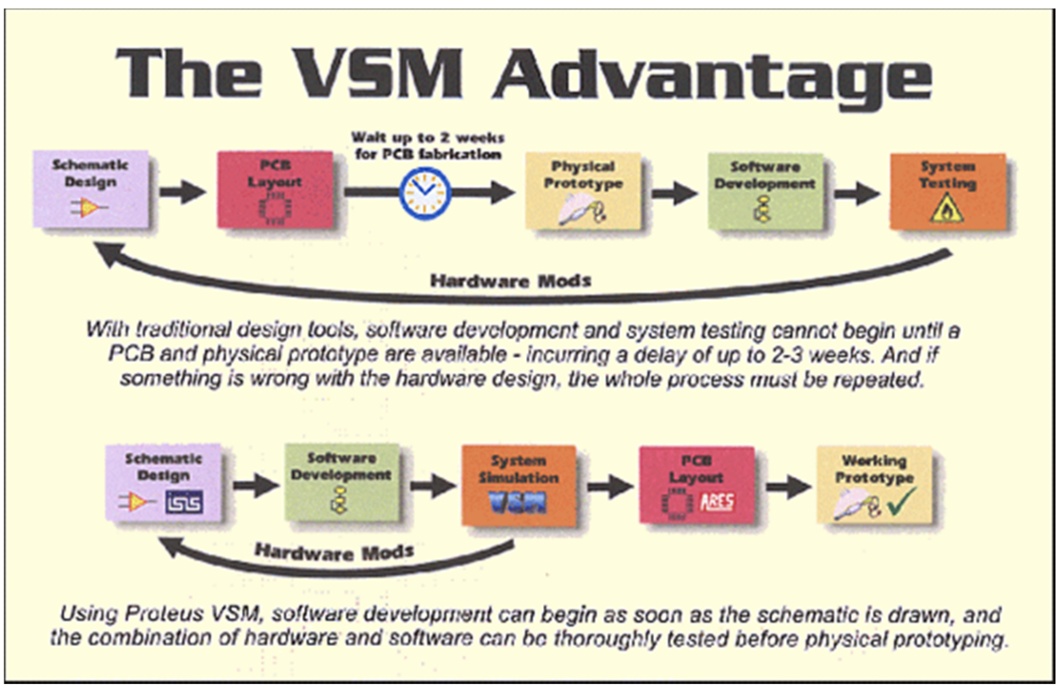

Figure 1.1

1.4.2.2 What is Proteus VSM?

Proteus Virtual System Modeling (VSM) combines mixed mode SPICE circuit simulation, animated components and microprocessor models to facilitate co-simulation of complete microcontroller based designs. For the first time ever, it is possible to develop and test such designs before a physical prototype is constructed.

This is possible because you can interact with the design using on screen indicators such as LED and LCD displays and actuators such as switches and buttons. The simulation takes place in real time (or near enough to it): a 1GMHz Pentium III can simulate a basic 8051 system clocking at over 12MHz. Proteus VSM also provides extensive debugging facilities including breakpoints, single stepping and variable display for both assembly code and high level language source.

1.4.2.3 Schematic Entry

Proteus VSM uses our proven Schematic Capture software to provide the environment for design entry and development. ISIS is a long established product and combines ease of use with powerful editing tools. It is capable of supporting schematic capture for both simulation and PCB design. Designs entered in to Proteus VSM for testing can be net listed for PCB layout either with our own PCB Design products or with third party PCB layout tools. ISIS also provides a very high degree of control over the drawing appearance, in terms of line widths, fill styles, fonts, etc. These capabilities are used to the full in providing the graphics necessary for circuit animation.

1.4.2.4 Circuit Simulation

At the heart of Proteus VSM is ProSPICE. This is an established product that combines uses a SPICE3f5 analogue simulator kernel with a fast event-driven digital simulator to provide seamless mixed-mode simulation. The use of a SPICE kernel lets you utilize any of the numerous manufacturer-supplied SPICE models now available and around 6000 of these are included with the package.

Proteus VSM includes a number of virtual instruments including an Oscilloscope, Logic Analyzer, Function Generator, Pattern Generator, Counter Timer and Virtual Terminal as well as simple voltmeters and ammeters. In addition, we provide dedicated Master/Slave/Monitor mode protocol analyzers for SPI and I2C - simply wire them onto the serial lines and monitor or interact with the data live during simulation. A truly invaluable (and inexpensive!) way to get your communication software right prior to hardware prototyping.

Should you wish to take detailed measurements on graphs, or perform other analysis types such as frequency, distortion, noise or sweep analyses of analogue circuits, you can purchase the Advanced Simulation Option. This option also includes Conformance Analysis - a unique and powerful tool for Software Quality Assurance.

1.4.2.5 Source Level Debugging

Whilst Proteus VSM is already unique in its capability to run near real time simulations of complete micro-controller systems, its real power comes from its ability to perform these simulations in single step mode. This works just like your favorite software debugger, except that as you single step the code, you can observe the effect on the entire design - including all the electronics external to the microcontroller

1.5 MAJOR COMPONENTS

1.5.1 PIC18F452 MICROCONTROLLER

PIC18F452 with high performance RISC CPU is used for processing the input. This powerful 10 MIPS (100 nanosecond instruction execution) yet easy-to-program (only 77 single word instructions) CMOS FLASH-based 8-bit microcontroller packs Microchip's powerful PIC® architecture into an 40- or 44-pin package and is upwards compatible with the PIC16C5X, PIC12CXXX, PIC16CXX and PIC17CXX devices and thus providing a seamless migration path of software code to higher levels of hardware integration. The PIC18F452 features a 'C' compiler friendly development environment, 256 bytes of EEPROM, Self-programming, an ICD, 2 capture/compare/PWM functions, 8 channels of 10-bit Analog-to-Digital (A/D) converter, the synchronous serial port can be configured as either 3-wire Serial Peripheral Interface (SPI™) or the 2-wire Inter-Integrated Circuit (I²C™) bus and Addressable Universal Asynchronous Receiver Transmitter (AUSART). All of these features make it ideal instrumentation and monitoring, data acquisition, power conditioning, environmental monitoring, telecom and consumer audio/video applications.

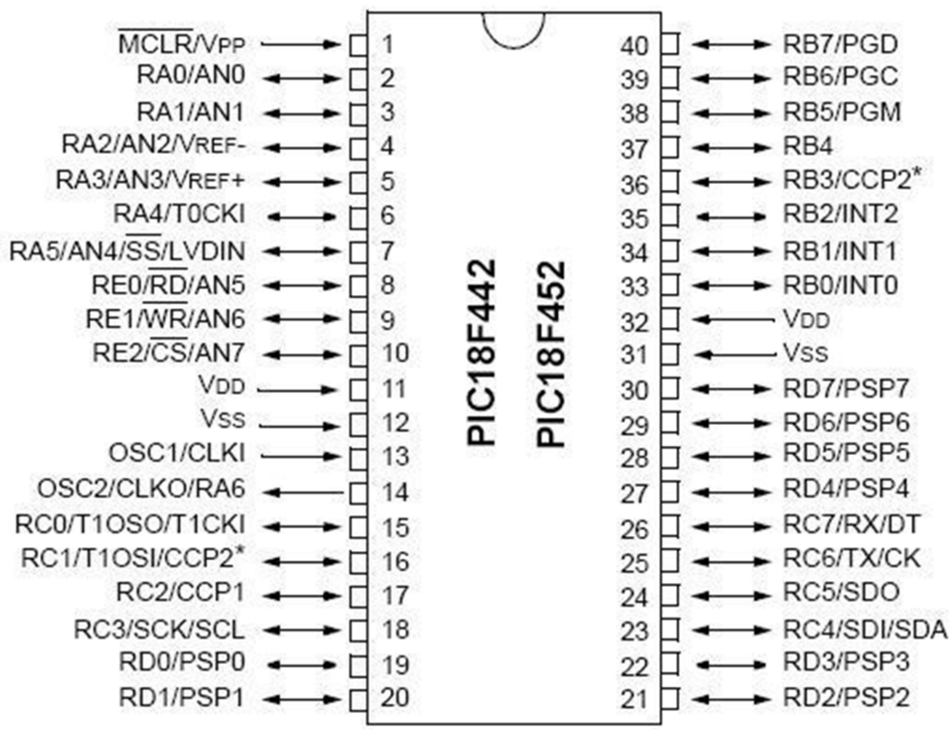

Figure 1.2

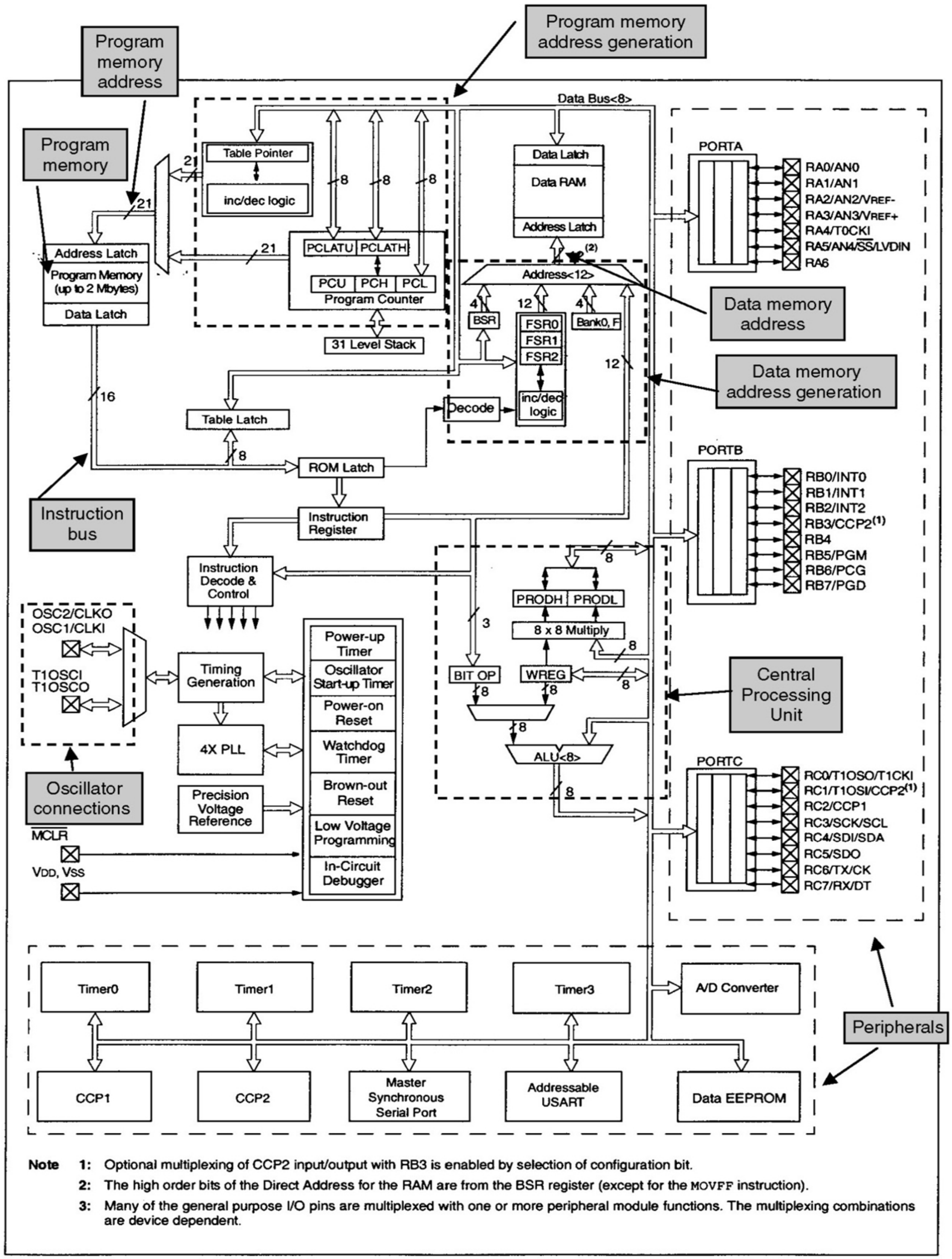
Program memory address generation
Program memory address
Program memory
Data Bus<8>
Table Pointer
inc/dec logic
PCLATU PCLATH
PCU PCH PCL
Program Counter
31 Level Stack
Address Latch
Program Memory (up to 2 Mbytes)
Data Latch
Data Latch
Data RAM
Address Latch
Address<12>
BSR
FSR0
FSR1
FSR2
inc/dec logic
Bank0, F
Decode
Data memory address
Data memory address generation
Table Latch
ROM Latch
Instruction Register
Instruction Decode & Control
Instruction bus
PORTA
RA0/AN0
RA1/AN1
RA2/AN2/VREF-
RA3/AN3/VREF+
RA4/T0CKI
RA5/AN4/SS/LVDIN
RA6
PORTB
RB0/INT0
RB1/INT1
RB2/INT2
RB3/CCP2(1)
RB4
RB5/PGM
RB6/PCG
RB7/PGD
PORTC
RC0/T1OSO/T1CKI
RC1/T1OSI/CCP2(1)
RC2/CCP1
RC3/SCK/SCL
RC4/SDI/SDA
RC5/SDO
RC6/TX/CK
RC7/RX/DT
PRODH PRODL
8 x 8 Multiply
BIT OP
WREG
ALU<8>
Central Processing Unit
OSC2/CLKO
OSC1/CLKI
T1OSCI
T1OSCO
Oscillator connections
Timing Generation
4X PLL
Precision Voltage Reference
Power-up Timer
Oscillator Start-up Timer
Power-on Reset
Watchdog Timer
Brown-out Reset
Low Voltage Programming
In-Circuit Debugger
MCLR
VDD, VSS
Timer0
Timer1
Timer2
Timer3
A/D Converter
CCP1
CCP2
Master Synchronous Serial Port
Addressable USART
Data EEPROM
Peripherals
Note 1: Optional multiplexing of CCP2 input/output with RB3 is enabled by selection of configuration bit.
2: The high order bits of the Direct Address for the RAM are from the BSR register (except for the MOVFF instruction).
3: Many of the general purpose I/O pins are multiplexed with one or more peripheral module functions. The multiplexing combinations are device dependent.

Figure 1.3

1.5.2 PC817A OPTOCOUPLER

There are many situations where signals and data need to be transferred from one subsystem to another within a piece of electronics equipment, or from one piece of equipment to another, without making a direct ohmic electrical connection. Often this is because the source and destination are (or may be at times) at very different voltage levels, like a microprocessor which is operating from 5V DC but being used to control a triac which is switching 240V AC. In such situations the link between the two must be an isolated one, to protect the microprocessor from overvoltage damage.

Relays can of course provide this kind of isolation, but even small relays tend to be fairly bulky compared with ICs and many of today's other miniature circuit components. Because they Are electro-mechanical, relays are also not as reliable — and only capable of relatively low speed operation. Where small size, higher speed and greater reliability are important, a much better alternative is to use an optocoupler. These use a beam of light to transmit the signals or data across an electrical barrier, and achieve excellent isolation.

Optocouplers typically come in a small 6-pin or 8-pin IC package, but are essentially a combination of two distinct devices: an optical transmitter, typically a gallium arsenide LED (light-emitting diode) and an optical receiver such as a phototransistor or light-triggered diac. The two are separated by a transparent barrier which blocks any electrical current flow between the two, but does allow the passage of light. The basic idea is shown in Fig.1, along with the usual circuit symbol for an optocoupler.

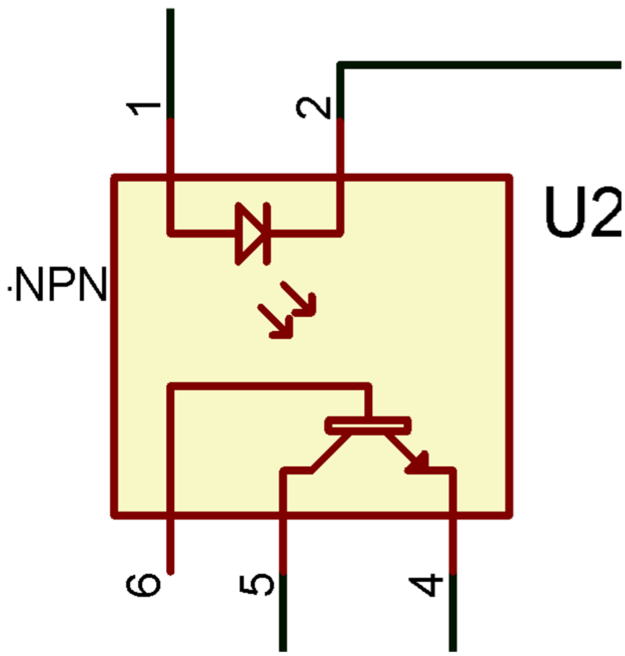

Figure 1.4

Usually the electrical connections to the LED section are brought out to the pins on one side of the package and those for the phototransistor or diac to the other side, to physically separate them as much as possible. This usually allows optocouplers to withstand voltages of anywhere between 500V and 7500V between input and output.

Optocouplers are essentially digital or switching devices, so they are best for transferring either on-off control signals or digital data. Analog signals can be transferred by means of frequency or pulse-width modulation.

Basically the simplest way to visualize an optocoupler is in terms of its two main components: the input LED and the output transistor or diac. As the two are electrically isolated, this gives a fair amount of flexibility when it comes to connecting them into circuit. All we really have to do is work out a convenient way of turning the input LED on and off, and using the resulting switching of the photo-transistor/diac to generate an output waveform or logic signal that is compatible with our output circuitry.

1.5.3 RELAY

A relay is an electrically operated switch. Many relays use an electromagnet to operate a switching mechanism mechanically, but other operating principles are also used. Relays are used where it is necessary to control a circuit by a low-power signal (with complete electrical isolation between control and controlled circuits), or where several circuits must be controlled by one signal. The first relays were used in long distance telegraph circuits, repeating the signal coming in from one circuit and re-transmitting it to another. Relays were used extensively in telephone exchanges and early computers to perform logical operations.

A type of relay that can handle the high power required to directly control an electric motor or other loads is called a contactor. Solid-state relays control power circuits with no moving parts, instead using a semiconductor device to perform switching. Relays with calibrated operating characteristics and sometimes multiple operating coils are used to protect electrical circuits from overload or faults; in modern electric power systems these functions are performed by digital instruments still called "protective relays".

Figure 1.5

1.5.4 LCD

LCD controller is one of the most common dot matrix liquid crystal display (LCD) display controllers available. Hitachi developed the microcontroller specifically to drive alphanumeric LCD display with a simple interface that could be connected to a general purpose microcontroller or microprocessor. Many manufacturers of displays integrated the controller with their product making it the informal standard for this type of displays. The device can display ASCII characters, Japanese Kana characters, and some symbols in two 28 character lines.

These LCD screens are limited to monochrome text and are often used in copiers, fax machines, laser printers, industrial test equipment, networking equipment such as routers and storage devices.

The screens come in a small number of standard configurations. Common sizes are 8x1 (one row of eight characters), 16×2, 20×2 and 20×4. Larger custom sizes are made with 32, 40 and 80 characters and with 1, 2, 4 or 8 lines. The most commonly manufactured larger configuration is 40×4 characters, which requires two individually addressable HD44780 controllers with expansion chips as a single HD44780 chip can only address up to 80 characters. A common smaller size is 16×2, and this size is readily available as surplus stock for hobbyist and prototyping work.

Character LCDs can come with or without backlights, which may be LED, fluorescent, or electroluminescent.

Character LCDs use a standard 16 contact interface, commonly using pins or card edge connections on 0.1 inch / 2.54mm centers. Those without backlights may have only 14 pins, omitting the final two pins powering the light. The pins are follows:

1. Ground
2. VCC (+3.3 to +5V)
3. Contrast adjustment (VO)
4. Register Select (RS). RS=0: Command, RS=1: Data
5. Read/Write (R/W). R/W=0: Write, R/W=1: Read
6. Clock (Enable). Falling edge triggered
7. Bit 0 (Not used in 4-bit operation)
8. Bit 1 (Not used in 4-bit operation)
9. Bit 2 (Not used in 4-bit operation)
10. Bit 3 (Not used in 4-bit operation)
11. Bit 4
12. Bit 5
13. Bit 6
14. Bit 7
15. Backlight Anode (+)

16. Backlight Cathode (-)

The nominal operating voltage for LED backlights is 5V at full brightness, with dimming at lower voltages dependent on the details such as LED color. Non-LED backlights often require higher voltages.

The HD44780 interface allows for two modes of operation, 8-bit and 4-bit. Using the 4 bit mode is more complex, but reduces the number of active connections needed. The chip starts in 8 bit mode, with the instruction set designed to allow switching without requiring the lower four data pins. Once in 4 bit mode, character and control data is transferred as pairs of 4 bit "nibbles" on the upper data pins, D4-D7.

Instruction	Code										Description	Execution time (max) (when f_{cp} = 270 kHz)
	RS	R/W	B7	B6	B5	B4	B3	B2	B1	B0		
Clear display	0	0	0	0	0	0	0	0	0	1	Clears display and returns cursor to the home position (address 0).	1.52 ms
Cursor home	0	0	0	0	0	0	0	0	1	*	Returns cursor to home position. Also returns display being shifted to the original position. DDRAM content remains unchanged.	1.52 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction (I/D); specifies to shift the display (S). These operations are performed during data read/write.	37 μs
Display on/off control	0	0	0	0	0	0	1	D	C	B	Sets on/off of all display (D), cursor on/off (C), and blink of cursor position character (B).	37 μs
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	*	*	Sets cursor-move or display-shift (S/C), shift direction (R/L). DDRAM content remains unchanged.	37 μs
Function set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display line (N), and character font (F).	37 μs
Set CGRAM address	0	0	0	1	CGRAM address						Sets the CGRAM address. CGRAM data are sent and received after this setting.	37 μs
Set DDRAM address	0	0	1	DDRAM address							Sets the DDRAM address. DDRAM data are sent and received after this setting.	37 μs
Read busy flag & address counter	0	1	BF	CGRAM/DDRAM address							Reads busy flag (BF) indicating internal operation being performed and reads CGRAM or DDRAM address counter contents (depending on previous instruction).	0 μs
Write CGRAM or DDRAM	1	0	Write Data								Write data to CGRAM or DDRAM.	37 μs
Read from CG/DDRAM	1	1	Read Data								Read data from CGRAM or DDRAM.	37 μs

Instruction bit names —

I/D - 0 = decrement cursor position, 1 = increment cursor position; **S** - 0 = no display shift, 1 = display shift; **D** - 0 = display off, 1 = display on; **C** - 0 = cursor off, 1 = cursor on; **B** - 0 = cursor blink off, 1 = cursor blink on ; **S/C** - 0 = move cursor, 1 = shift display; **R/L** - 0 = shift left, 1 = shift right; **DL** - 0 = 4-bit interface, 1 = 8-bit interface; **N** - 0 = 1/8 or 1/11 duty (1 line), 1 = 1/16 duty (2 lines); **F** - 0 = 5×8 dots, 1 = 5×10 dots; **BF** - can accept instruction, 1 = internal operation in progress.

1.5.5 CIRCUIT DIAGRAM

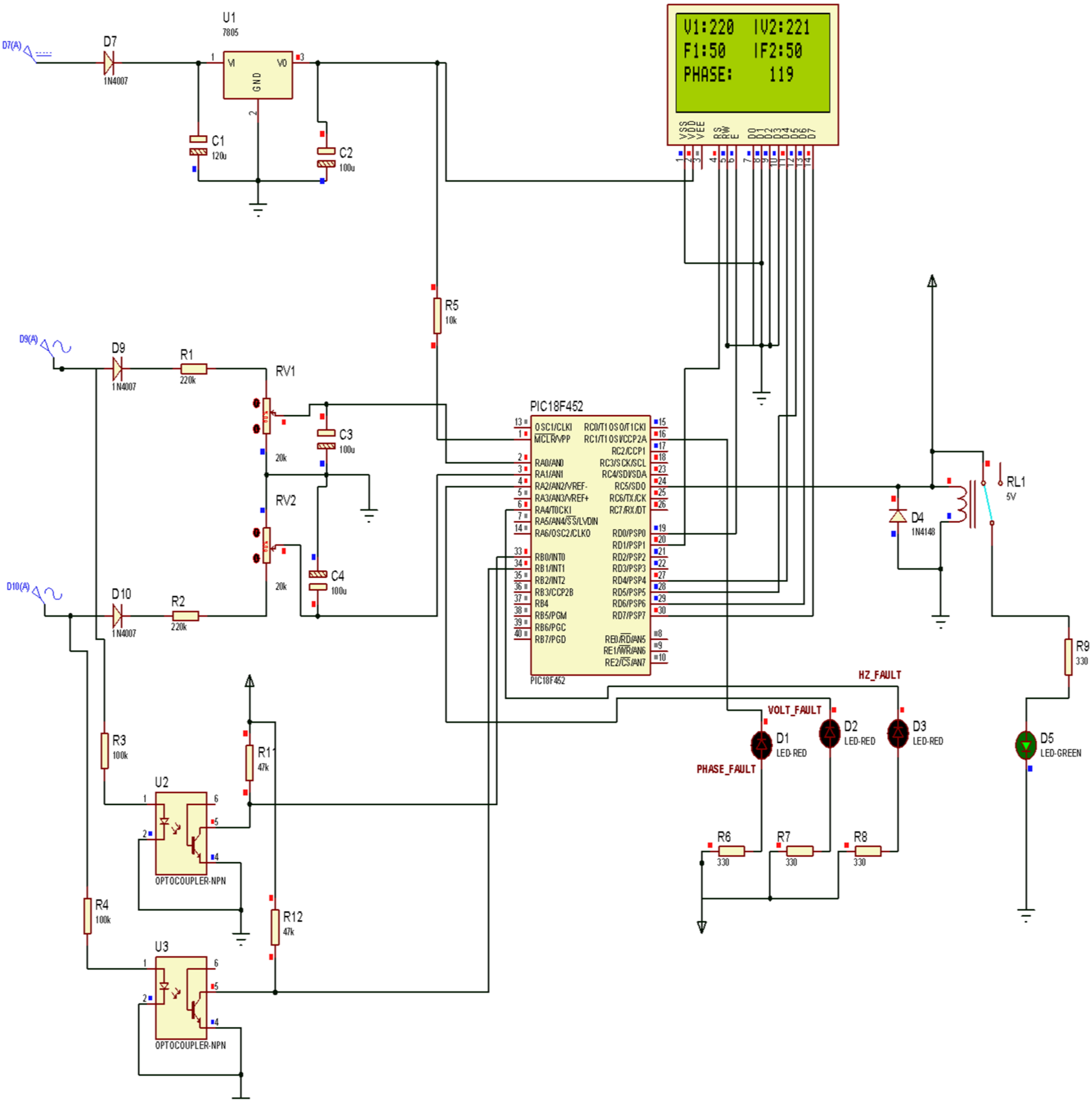

Figure 1.6